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FPGA Implementation Of Efficient Modified VLSI Architecture For Multiplier

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Abstract:- The multiplication operation is present in many parts of a digital system or digital computer and also in signal processing, graphics and scientific computation. With advances in various technologies, various techniques have been proposed to design multipliers, with high speed, low power consumption and lesser area. Various high speed low power compact VLSI implementations are possible only with multipliers. This project presents a high-speed and low area 16×16 bit Modified Booth Multiplier (MBM) with Carry Select Adder (CSA) and 3-stage pipelining technique. These techniques to improve the performance by reducing the time delay. These multiplication techniques are design using hardware description language (HDL) and it can simulate using modelsim software and also it will implement in Spartan 3E FPGA and also power consumption will estimate using tanner EDA tool.

Keywords:-Carry select adder (CSA), 3-stage pipelining, Modified Booth Multiplier, Xilinx ISE 9.1, Tanner tool EDA

I.INTRODUCTION

Nowadays electronic equipments play a very vital role, like in mobile phone, laptops, tablets etc. These devices operate on their internal processor, RAM and hard disk. Binary and various arithmetic operations are performed by processor. The demand of fast processors is increasing for high-speed data processing. The multipliers are the better option for high-speed data processing. In this paper, Carry Select Adder (CSA) with 3-stage pipelining technique is used for enhancing the performance and reducing the area of Modified Booth Multiplier (MBM).

The architecture of Modified Booth Multiplier consists of 3-stages. First stage includes booth encoder and decoder circuit. Second stage includes Wallace tree structure which is composed of unit adders and the last stage is composed of CSA. CSA is consists of two sections, one for higher order bits and other for low order bits. Selection of adder is based on Cin. Any improvement in each section may improve the multiplier performance. As the number of stages increases, the power consumption and area gets increased. This drawback can be overcome by using CSA with 3-stage pipeline technique. The block diagram of MBM using CSA and pipelining

II.PARTIAL PRODUCT GENERATION

In an n-bit modified Booth multiplier, the number of Booth encoders is n/2 and the number of partial product generator (PPG) circuits is approximately n^2 , hence power consumption and die area in the Booth section is dominated by PPG. So, integration of PPG (Booth Decoder) section is more important than Booth encoder (BE) block. The conventionally used modified Booth selector computes the partial product of jth bit and ith row by using the equation1.

$$PPij=(Xj.X1\_2+Xj-1.X1\_1)XOR\ Neg \quad (1)$$

Where Xj and Xj-1 are the multiplicand inputs of weight 2j and 2j-1 respectively, X1_2 and X1_1 determine whether the multiplicand should be doubled or not and Neg is a digit which determines if the multiplicand should be inverted or not.

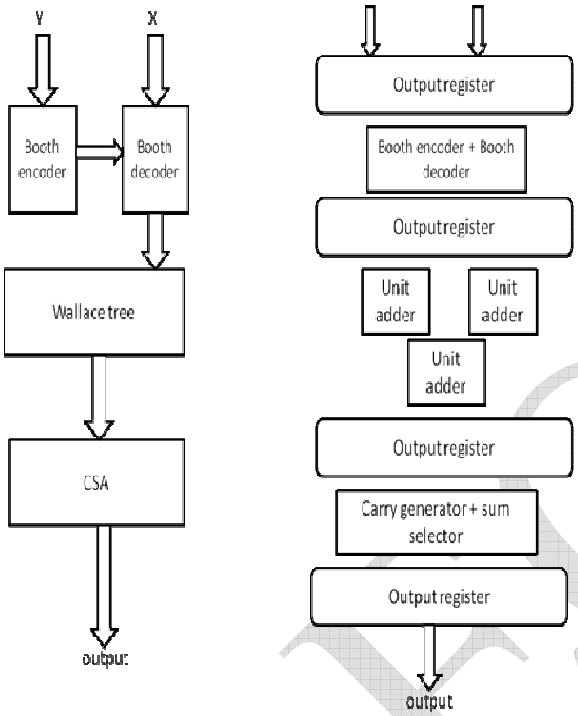


Fig 1: Block Diagram of Modified Booth Multiplier

III.WALLACE TREE MULTIPLIER

A fast process for multiplication of two numbers was developed by Wallace. Wallace observed that it is possible to find a structure, which performs the addition operations in parallel, resulting in less delay. Wallace introduced a different way of parallel addition of the partial product bits using a tree of carry save adders, which is known as "Wallace Tree". A Wallace tree is an efficient hardware implementation of a digital circuit that multiplies two integers. In order to perform the multiplication of two numbers with the Wallace method, partial product matrix is reduced to a two-row matrix by using a carry save adder, and the remaining two rows are summed using a fast carry- save adder to form the product.

Addition of partial products will increase the speed of Wallace Tree multiplier. In Wallace Tree architecture, all the bits of all of the partial products in each column are added together by a set of counters in parallel without propagating any carries. Another set of counters then reduces this new matrix and so on, until a two-row matrix is generated.

Wallace tree multiplier performs the following operations:

- Formation of bit products.
- The bit product matrix is reduced to a 2-row matrix by using a carry-save adder.
- The remaining two rows are summed using a fast carry-propagate adder to Produce the product.

A. Carry Save Adder

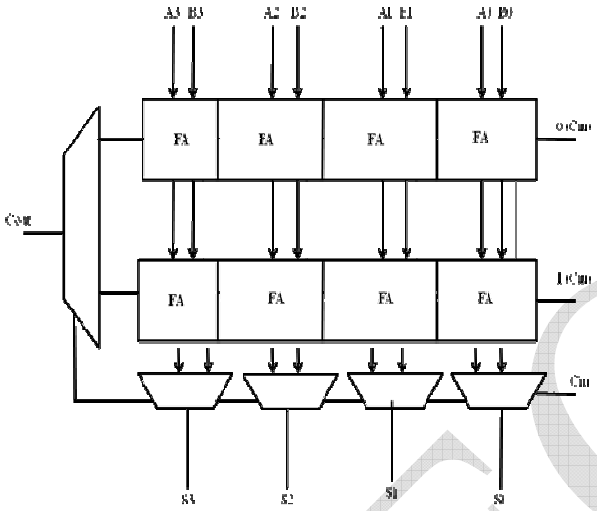
Carry Save Adder performs the addition of "m" numbers in faster than normal or regular addition. A carry save adder consist of full adders like ripple carry adders, but the carry output from each bit is taken out to form second result vector rather than being wired to the next most significant bit. It takes three numbers (a, b, c) to add together and output two numbers, sum (s) and carry (c). It is carried out in one time unit duration. In carry-save adder, the carry (c) is bought until the last step and the ordinary addition is carried out in the very last step.

The most important application of a carry-save adder is to calculate the partial products in integer multiplication. This allows for architectures, where a tree of carry- save adders (also called Wallace tree) is used to calculate the partial products very fast.

B. Advantage of Wallace Multiplier

Propagation delay of this multiplier is ($\log_{a/2}(N)$), it is reduced compare with array multiplier.

IV.CARRY-SELECT ADDER



The carry-select adder generally consists of two ripple carry adder and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known.

V. COMPARISON RESULTS BETWEEN CSA & CLA

Logic utilization	**CLA**	**CSA**	**Per. reduction**
No.of.slice	**394**	**377**	**4.3%**
No.of.LUTs	**749**	**718**	**4.1%**
Delay in ns	**51.92**	**22.38**	**56.8%**

VI.CONCLUTION

From this paper, we have designed modified booth multiplier by using of three stage pipelining technique. In this paper's idea, this architecture is more efficient and the designed MBM having low power, less area and high speed and also efficient for VLSI hardware implementation.

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